MOTOROLA

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19 **Number of Pages (Including this page)**

**Date:** September 27, 2004

**To:** Examiner Abraham, E. – Group 2133

**Location:** United States Patent and Trademark Office

**Fax No.:** 703-872-9306

**From:** Steven A. May (Registration No. 44,912)

**Subject:** Serial No. 09/775,950 –Chen et al.

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MESSAGE:

Enclosed herewith, please find a APPEAL BRIEF UNDER 37 CFR 1.192 for filing in the below-identified application.

## PLEASE GIVE THESE PAPERS TO:

| | |
|---|---|
| EXAMINER: | **Abraham, E.** |
| GROUP ART UNIT: | 2133 |
| SERIAL NO.: | 09/775,950 |
| FILED: | January 18, 2001 |
| INVENTOR: | Chen et al. |
| ATTORNEY DOCKET NO.: | CE08674R |

PTO/SB/21 (08-00)

# TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in this Submission: 4

| | |
|---|---|
| Application Number | 09/775,950 |
| Filing Date | January 18, 2001 |
| First Named Inventor | Chen et al. |
| Group Art Unit | 2133 |
| Examiner Name | Abraham, E. |
| Attorney Docket Number | CE08674R |

## ENCLOSURES (check all that apply)

- [X] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/Declaration(s)
- [ ] Extension of time Request
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- [ ] Response to Missing Parts Under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers (for an Application)
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- [ ] Licensing-Related papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation, Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CDs
- [ ] After Allowance Communication to Group
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- [X] Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
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Remarks

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | | | |
|---|---|---|---|
| Firm or Individual | Steven A. May | Registration No. | 44,912 |
| Signature | | | |
| Date | September 27, 2004 | | |

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| | | | |
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| Typed or printed name | Nanette Orr | | |
| Signature | | Date | September 27, 2004 |

# FEE TRANSMITTAL

Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT ($)

| Complete If Known | |
|---|---|
| Application Number | 09/775,950 |
| Filing Date | January 18, 2001 |
| First Named Inventor | Chen et al. |
| Examiner Name | Abraham, E. |
| Group Art Unit | 2133 |
| Attorney Docket No. | CE08674R |

## METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayment to:

Deposit Account Number: 50-2117

Deposit Account Name: Motorola, Inc.

[X] Charge Any Additional Fee required under 37 CFR 1.16 and 1.17

[ ] Applicant claims small entity status. See 37 CFR 1.27

2. [ ] Payment Enclosed:

[ ] Check [ ] Credit Card [ ] Money Order [ ] Other

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | | Fee Paid |
|---|---|---|---|---|---|
| 1001 | 750 | 2001 | 375 | Utility filing fee | |
| 1002 | 330 | 2002 | 165 | Design filing fee | |
| 1003 | 520 | 2003 | 260 | Plant filing fee | |
| 1004 | 750 | 2004 | 375 | Reissue filing fee | |
| 1005 | 160 | 2005 | 80 | Provisional filing fee | |

SUBTOTAL (1) ($) 0.00

### 2. EXTRA CLAIM FEES

| | | Previously Paid** | | Extra Claims | | Fee from below | | Fee Paid |
|---|---|---|---|---|---|---|---|---|
| Total Claims | | 20 | = | | X | 18 | = | |
| Independent Claims | | 3 | = | | X | 84 | = | |
| Multiple Dependent | | | | | | 280 | = | |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 84 | 2201 | 42 | Independent claims in excess of 3 |
| 1203 | 280 | 2203 | 140 | Multiple dependent claim, if not paid |
| 1204 | 84 | 2204 | 42 | * Reissue independent claims over original patent |
| 1205 | 18 | 2205 | 9 | *Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($) 0.00

**OR NUMBER PREVIOUSLY PAID, IF GREATER THAN STANDARD ALLOWANCE.
*For Reissues, see above

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge – late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge – late Provisional filing | |
| 1053 | 130 | 1053 | 130 | Non-English specification | |
| 1812 | 2520 | 1812 | 2520 | For filing a request for ex parte Reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1840* | 1805 | 1840* | Requesting publication of SIR after Examiner action | |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | |
| 1252 | 410 | 2252 | 205 | Extension for reply within second month | |
| 1253 | 930 | 2253 | 465 | Extension for reply within third month | |
| 1254 | 1450 | 2254 | 725 | Extension for reply within fourth month | |
| 1255 | 1970 | 2255 | 985 | Extension for reply within fifth month | |
| 1401 | 320 | 2401 | 160 | Notice of Appeal | |
| 1402 | 320 | 2402 | 160 | Filing a brief in support of an appeal | |
| 1403 | 280 | 2403 | 140 | Request for oral hearing | |
| 1451 | 1510 | 1451 | 1510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive - unavoidable | |
| 1453 | 1300 | 2453 | 650 | Petition to revive - unintentional | |
| 1501 | 1300 | 2501 | 650 | Utility issue fee (or reissue) | |
| 1502 | 470 | 2502 | 235 | Design issue fee | |
| 1503 | 630 | 2503 | 315 | Plant issue fee | |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | |
| 1807 | 50 | 1807 | 50 | Processing fee under 37 CFR 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of IDS | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 750 | 2809 | 375 | Filing a submission after final rejection (37 CFR § 1.129(a)) | |
| 1810 | 750 | 2810 | 375 | For each additional invention to be examined (37 CFR § 1.129(b)) | |
| 1801 (RCE) | 750 | 2801 | 375 | Request for Continued Examination | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify)

* Reduced by Basic Filing Fee paid SUBTOTAL (3) ($)

## SUBMITTED BY

Complete (if applicable)

| Name (Print/Type) | Steven A. May | Registration No. | 44,912 | Telephone | (847) 576-3635 |
|---|---|---|---|---|---|
| Signature | | Date | September 27, 2004 | | |

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- PATENT -

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| APPLICANT: | Chen | EXAMINER: | Abraham, E. |
| SERIAL NO.: | 09/775,950 | ART UNIT: | 2133 |
| FILED: | 01/18/01 | CASE NO.: | CE08674R |
| ENTITLED: | APPARATUS AND METHOD FOR PROVIDING TURBO CODE INTERLEAVING IN A COMMUNICATIONS SYSTEM | | |

Motorola, Inc.
Corporate Offices
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September 27, 2004

**APPEAL BRIEF UNDER 37 CFR 1.192**

Certificate of Transmission under 37 CFR 1.8

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on September 27, 2004

Motorola, Inc.
Name of applicant, assignee, or Registered Representative

9/27/2004
Date

Signature

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Commissioner:

The appellant hereby respectfully submits the following Appeal Brief in response to a Final Office Action dated March 3, 2004, and a Notice of Appeal filed July 27, 2004.

1. REAL PARTY IN INTEREST

The real party in interest in this appeal is Motorola, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

3. STATUS OF CLAIMS

This is an appeal from a Final Office Action, dated March 3, 2004. Claims 1-19 are appealed. In a first Office Action dated September 9, 2003, the Examiner objected to claim 7 based on an informality. The Examiner rejected claims 1-6 under 35 U.S.C. §101 as being directed to an algorithm and not embedded in a computer readable medium. The Examiner rejected claims 7-19 under 35 U.S.C. §103(a) as being unpatentable over Eroz et al. (U.S. patent no. 6,334,197, hereinafter referred to as "Eroz").

In an Amendment dated February 9, 2004, the appellants amended claim 7 to correct the informality and responded to the rejections of claims 1-19.

In the Final Office Action, dated March 3, 2004, the Examiner rejected claims 1-6 under 35 U.S.C. §101 as being directed to an algorithm and not embedded in a computer readable medium. The Examiner rejected claims 7-19 under 35 U.S.C. §103(a) as being unpatentable over Eroz.

A Response to the Final Office Action was filed on July 27, 2004, and is currently pending. In the Response to the Final Office Action, the appellants amended claim 1 in accordance with a suggestion of the Examiner to direct the claim to an interleaving method for interleaving data elements in a communication system employing turbo codes. No other claims were amended. The appellants further responded to the Examiner's rejections of claims 1-19. Claim 1, as amended, is merely a method format of the interleavers disclosed by claims 7 and 14. Therefore, the appellants contend that the claim 1, as amended, does not necessitate a new search and properly may be considered in this appeal.

Claim 1, as amended, provides an interleaving method for interleaving data elements in a communication system employing turbo codes. The method includes writing address locations of the data elements sequentially by rows into a matrix having a predetermined number of bit storage locations arranged in a first predetermined number of rows having corresponding row indexes and a second predetermined number of columns having corresponding column indexes. The method further includes bit reversing the row indexes for the first predetermined number of rows and permuting the corresponding address locations of the data elements, bit reversing the column indexes for the second predetermined number of columns and permuting the corresponding address locations of the data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns.

Claim 7, as amended, provides an interleaver that includes an input device, a controller, and an output device. The input device is configured to write addresses of elements stored in an input memory sequentially by rows into a matrix of at least a predetermined number of bit storage locations having a first predetermined number of rows and a second predetermined number of columns. The controller is configured to bit reverse row indexes for the first predetermined number of rows and permute the corresponding data elements, bit reverse column indexes for the second predetermined number of columns and permute the corresponding data elements, and shift bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns.

Claim 13 provides a data transmission system employing turbo encoding. The system includes a turbo encoder having multiple coders for coding received data frames and an interleaver located between an input to the turbo encoder and one of the multiple coders. The interleaver is configured to interleave address locations of bits within a matrix having a first predetermined number of rows and a second predetermined number of columns by bit reversing row indexes for the first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for the second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a

respective predetermined number of columns. The system further includes a decoder configured to receive and decode the turbo encoded data frames.

Claim 14 provides an interleaver having an input data memory, an interleaver matrix, a controller, an output buffer, and an output memory. The input data memory is configured to store an *N* number of bits at corresponding input data memory addresses. The interleaver matrix is configured to read and store the input data memory addresses in at least a two-dimensional matrix having a first predetermined number of rows and a second predetermined number of columns, each of the rows and columns having an assigned index value. The controller is configured to set the first predetermined number of rows and the second predetermined number of rows based on the *N* number of bits using a prescribed algorithm, to interleave the data memory address in the interleaver matrix by bit reversing the row index values for the first predetermined number of rows and permuting the corresponding address locations of the data elements, bit reversing the column index values for the second predetermined number of columns and permuting the corresponding address locations of the data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns, and to read out interleaved data bit addresses in the interleaver matrix column by column to produce an interleaved output read sequence.

No Advisory Action has been received by the applicants. No claims have been allowed. The pending claims 1-19 are reproduced below in the attached Appendix.

## 4. STATUS OF AMENDMENTS

A Response to the Final Office Action was filed on July 27, 2004, and is currently pending. In the Response to the Final Office Action, the appellants amended claim 1 in accordance with a suggestion of the Examiner to direct the claim to an interleaving method for interleaving data elements in a communication system employing turbo codes. Also, the appellants responded to the Examiner's rejections of claims 1-19. However, as noted above, claim 1, as amended, is merely a method format of the interleavers disclosed by claims 7 and 14. Therefore, the appellants contend that the method disclosed by claim 1, as amended, was already disclosed with respect to the claimed interleavers of claims 7

and 14, does not necessitate a new search, and properly may be considered in this appeal. No Advisory Action has been received.

## 5. SUMMARY OF INVENTION

The appellant's invention provides a communication system that employs turbo encoding, the system having a more easily implemented turbo interleaver that interleaves input data efficiently with little use of system resources and that does not require look-up tables. The turbo interleaver reads address locations of the data bits into an interleaver matrix array row by row and interleaves the address locations by bit reversal of the row indexes with accompanying permutation of the corresponding address locations in the rows of the matrix, bit reversal of the column indexes with accompanying permutation of the corresponding address locations in the columns of the matrix and shifting the address locations within each row a predetermined number of column locations based on the particular row number.

Claim 1, as amended, provided an interleaving method for interleaving data elements in a communication system employing turbo codes. The method includes steps of writing address locations of the data elements sequentially by rows into a matrix having a predetermined number of bit storage locations arranged in a first predetermined number of rows having corresponding row indexes and a second predetermined number of columns having corresponding column indexes. The method further includes steps of bit reversing the row indexes for the first predetermined number of rows and permuting the corresponding address locations of the data elements, bit reversing the column indexes for the second predetermined number of columns and permuting the corresponding address locations of the data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. (Figures 2 and 4; page 4, line 19 to page 5, line 23; page 6, line 8 to page 7, line 13; page 10, line 4 to page 11, line 25)

Claim 7, as amended, provided an interleaver that includes an input device configured for receiving and temporarily storing data elements in an input memory, the input device also configured to write addresses of the elements in the input memory

sequentially by rows into a matrix of at least a predetermined number of bit storage locations having a first predetermined number of rows and a second predetermined number of columns. The interleaver further includes a controller configured to bit reverse row indexes for the first predetermined number of rows and permute the corresponding data elements, bit reverse column indexes for the second predetermined number of columns and permute the corresponding data elements, and shift bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. The interleaver further includes an output device configured to sequentially read the interleaved input memory addresses from the columns of the matrix and read and transmit data elements stored at corresponding memory addresses in the sequential read order of the interleaved input memory addresses. (Figures 2, 3, and 4; page 4, line 19 to page 5, line 23; page 6, line 8 to page 7, line 13; page 8, line 10 to page 11, line 25)

Claim 13 provided a data transmission system employing turbo encoding. The system includes a turbo encoder for turbo encoding received data frames and transmitting the encoded data frames within the data transmission system, the turbo encoder including multiple coders for coding the received data frame and an interleaver located between an input to the turbo encoder and one of the multiple coders. The interleaver is configured to interleave address locations of bits within a matrix having a first predetermined number of rows and a second predetermined number of columns by bit reversing row indexes for the first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for the second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. The system further includes a decoder configured to receive and decode the turbo encoded data frames transmitted by the turbo encoder, the decoder including a de-interleaver that receives the interleaved reassembles the address locations of bits within the matrix by reversing the interleaved output of the interleaver using reverse steps of the interleaver. (Figures 1-5; page 3, line 25 to page 4, line 7; page 4, line 19 to page 5, line 23; page 6, line 8 to page 7, line 13; page 8, line 10 to page 12, line 12)

Claim 14 provided an interleaver. The interleaver included an input data memory configured to store an *N* number of bits at corresponding input data memory addresses, and an interleaver matrix configured to read and store the input data memory addresses in at least a two-dimensional matrix having a first predetermined number of rows and a second predetermined number of columns, each of the rows and columns having an assigned index value. The interleaver further includes a controller configured to set the first predetermined number of rows and the second predetermined number of rows based on the *N* number of bits using a prescribed algorithm. The controller is further configured to interleave the data memory address in the interleaver matrix by bit reversing the row index values for the first predetermined number of rows and permuting the corresponding address locations of the data elements, bit reversing the column index values for the second predetermined number of columns and permuting the corresponding address locations of the data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. The controller is further configured to read out interleaved data bit addresses in the interleaver matrix column by column to produce an interleaved output read sequence. The interleaver further includes an output buffer that receives the interleaved output read sequence from the controller, the output buffer configured to direct the input data memory to read out data bit according to the interleaved output read sequence, and an output data memory configured to write data bits read out from the input data memory according to the interleaved output read sequence and transmit the read bits to a communication system. (Figures 2, 3, and 4; page 4, line 19 to page 7, line 13; page 8, line 10 to page 11, line 25)

6. ISSUES

**Issue 1**

Whether claim 1 is unpatentable under 35 U.S.C. §101 as being directed to an algorithm and not embedded in a computer readable medium.

**Issue 2**

Whether claims 7, 13, and 14 are unpatentable under 35 U.S.C. §103(a) over Eroz.

7. GROUPING OF CLAIMS

Appellants designate the following groups of claims:

Group I: claims 1-6;

Group II: claims 7-19.

8. ARGUMENT

(i) Rejection under 35 U.S.C. §112, first paragraph:

None

(ii) Rejection under 35 U.S.C. §112, second paragraph:

None

(iii) Rejection under 35 U.S.C. §102:

None

(iv) Rejection under 35 U.S.C. §103:

The Examiner rejected claims 7-19 under 35 U.S.C. §103(a) as being unpatentable over Eroz. Specifically, with respect to claims 7, 13, and 14, the Examiner contended that Eroz teaches a two dimensional block interleaver (element 16 in FIG. 2) comprising a number of rows and a number of columns, wherein data is read into the interleaver row-by-row, then row and column permutations are performed to randomize data positions, and then the data is read out column-by-column (col. 9, lines 2-10). Specifically, the Examiner noted that Eroz teaches for an input position '$1 = C * i + j$,' a corresponding output position is '$I(1) = R*\Pi_i(j) + \rho(i)$,' where '$\Pi_i$' is a column permutation application to data in row I and '$\rho$' is bit reversed indexing (col. 9, lines 11-17). The Examiner acknowledged that Eroz does not disclose a controller configured to bit reverse row and column indices. However, the Examiner contended that it would have been well known to one of ordinary skill in the art that controllers are required in order to perform read and write operations for forward or backward (bit reversing) operations.

The appellants respectfully disagree with the Examiner's interpretation of Eroz. In the interleaver of Eroz, for an input position '$1 = C * i + j$,' a corresponding output position is '$I(1) = R*\Pi_i(j) + \rho(i)$,' where '$\rho(i)$' is the bit reversal pattern for the $i^{th}$ row and '$\Pi_i(j)$' is a column permutation applied to the data in the $i^{th}$ row. While '$\Pi_i(j)$' is a column permutation pattern, it is not done with bit reversals for the columns as in claims 7, 13, and 14. Instead, Eroz implements the column permutation pattern by use of Galois field arithmetic, which is extremely difficult to implement and which results in a totally different pattern than the bit reversal indexing of claims 7, 13, and 14. Furthermore, while Eroz provides a bit reversal index '$\rho(i)$' for each row, each of claims 7, 13, and 14 goes beyond Eroz by providing a row shifting operation for each row with a specific pattern after bit reversal indexing.

Therefore, it is no surprise that the relationship between the starting interleaver matrix (the matrix on page 6, line 12 of the pending application and matrix 8 in Eroz) and the final interleaver matrix (the matrix on page 7, line 9 of the pending application and matrix 17 in Eroz) is completely different between the pending application and Eroz and results in different final distances of adjacent input values, as the interleaver of claims 7, 13, and 14 use bit-reversal combined with a shifting operation that results in a completely different distribution of the transmitted bits. Eroz does not teach the features of claims 7, 13, and 14 of bit reversing row indexes for a first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for a second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. Accordingly, the appellants respectfully submit that claims 7, 13, and 14 are not unpatentable over the prior art of record.

Regarding dependent claims 8-12 and 15-19, because claims 8-12 depend directly or indirectly from independent claim 7 and claims 15-19 depend directly or indirectly from independent claim 14, the appellants respectfully submit that claims 8-12 and 15-19 are not unpatentable over the prior art of record.

Although claim 1 has not been rejected under Eroz, the appellants contend that claim 1, as amended by the appellants' Response to the Final Office Action, also is not

unpatentable over the prior art of record. Claim 1, as amended, teaches a method of interleaving that includes bit reversing the row indexes for a first predetermined number of rows and permuting the corresponding address locations of the data elements, bit reversing the column indexes for the second predetermined number of columns and permuting the corresponding address locations of the data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. As noted above, these features are not taught by Eroz. Accordingly, the appellants respectfully submit that claim 1, as amended, is not unpatentable over the prior art of record.

Since claims 2-6 depend directly or indirectly from independent claim 1, the appellants further contend that claims 2-6 also are not unpatentable over the prior art of record.

(v) Other rejections

The Examiner rejected claims 1-6 under 35 U.S.C. §101 as being directed to an algorithm and not embedded in a computer readable medium, noting that the steps therein are directed to mathematical algorithms rather than limited to practical applications. In accordance with a suggestion of the Examiner, in their Response to the Final Office Action the appellants amended claim 1 to direct the claim to an interleaving method for interleaving data elements in a communication system employing turbo codes. The method disclosed by claim 1, as amended, is merely a method format of the interleavers disclosed by claims 7 and 14. Therefore, the appellants contend that the method disclosed by claim 1, as amended, was already disclosed with respect to the claimed interleavers of claims 7 and 14, does not necessitate a new search, and properly may be considered in this appeal. Accordingly, the appellants respectfully submit that claim 1 is no longer directed to an algorithm rather than a practical application and, as amended, is not unpatentable under 35 U.S.C. §101.

8. CONCLUSION

For the above reasons, the appellant respectfully submits that the rejection of claims 1-6 under 35 U.S.C. §101 as being an unpatentable algorithm and the rejection of

claims 7-19 under 35 U.S.C. §103(a) as being unpatentable over Eroz is in error and should be reversed and the claims allowed.

Respectfully submitted,
Jiangnan Chen

By: _____

Steven A. May
Attorney for Applicants
Registration No. 44,912
Phone No.: 847/576-3635
Fax No.: 847/576-3750

## APPENDIX

1. An interleaving method for interleaving data elements in a communication system employing turbo codes, the method comprising the steps of:

writing address locations of the data elements sequentially by rows into a matrix having a predetermined number of bit storage locations arranged in a first predetermined number of rows having corresponding row indexes and a second predetermined number of columns having corresponding column indexes;

bit reversing the row indexes for the first predetermined number of rows and permuting the corresponding address locations of the data elements;

bit reversing the column indexes for the second predetermined number of columns and permuting the corresponding address locations of the data elements; and

shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns.

2. The method according to claim 1, further comprising the steps of:

determining an $N$ number of bits within a frame to be transmitted and setting the predetermined number of bit storage locations equal to $N$; and

setting the first predetermined number of rows and second predetermined number of columns to $2^m$ and $2^n$, respectively, where the values $m$ and $n$ are set such that $2^{n+m}$ is greater than or equal to $N$.

3. The method according to claim 2, wherein the values of $m$ and $n$ are set such that $n$ is greater than or equal to $m$ and that the absolute value of the difference of values $m$ and $n$ is less than or equal to one.

4. The method according to claim 1, further comprising the step of reading the data elements out of the matrix column by column starting with a first column after the columns have been reversed and the rows have been reversed and shifted.

5. The method according to claim 1, wherein the steps of reversing bit storage locations for the first predetermined number of rows, reversing bit storage locations for the second

predetermined number of columns, and shifting bit storage locations of each of the second predetermined number of rows a respective predetermined number of columns are performed for each data element when each individual data element is written to the matrix.

6. The method according to claim 2, wherein data elements in each particular row of the matrix are each shifted in a predetermined direction within the matrix a specified number of columns as determined by the relationship $2^m$ - (row# - 1), where row# is a number of the particular row in the matrix and $2^m$ is the total number of rows in the matrix.

7. An interleaver comprising:

an input device configured for receiving and temporarily storing data elements in an input memory, the input device also configured to write addresses of the elements in the input memory sequentially by rows into a matrix of at least a predetermined number of bit storage locations having a first predetermined number of rows and a second predetermined number of columns;

a controller configured to bit reverse row indexes for the first predetermined number of rows and permute the corresponding data elements, bit reverse column indexes for the second predetermined number of columns and permute the corresponding data elements, and shift bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns; and

an output device configured to sequentially read the interleaved input memory addresses from the columns of the matrix and read and transmit data elements stored at corresponding memory addresses in the sequential read order of the interleaved input memory addresses.

8. The interleaver according to claim 7, wherein the controller is further configured to:

determine an $N$ number of bits within a frame to be transmitted;

set the predetermined number of bit storage locations equal to $N$; and

set the first predetermined number of rows and second predetermined number of columns to $2^m$ and $2^n$, respectively, where the values $m$ and $n$ are set such that $2^{n+m}$ is greater than or equal to the at least $N$ number of bit storage locations.

9. The interleaver according to claim 8, wherein the values of $m$ and $n$ are set such that $n$ is greater than or equal to $m$ and that the absolute value of the difference of values $m$ and $n$ is less than or equal to one.

10. The interleaver according to claim 7, wherein the output device sequentially reads the data elements out of the matrix column by column starting with a first column.

11. The interleaver according to claim 7, wherein the controller is configured to reverse the bit storage locations for the first predetermined number of rows, reverse the bit storage locations for the second predetermined number of columns, and shift the bit storage locations of each of the second predetermined number of rows a respective predetermined number of columns for each data element when each individual data element is written to the matrix.

12. The interleaver according to claim 7, wherein the controller is configured to shift data elements in each particular row of the matrix a predetermined direction within the matrix a specified number of columns as determined by the relationship $2^m$ - (row#-1), where row# is a number of the particular row in the matrix and $2^m$ is the total number of rows in the matrix.

13. A data transmission system employing turbo encoding comprising:

a turbo encoder for turbo encoding received data frames and transmitting the encoded data frames within the data transmission system, the turbo encoder including:

a plurality of coders for coding the received data frame; and

an interleaver located between an input to the turbo encoder and one of the plurality of coder, the interleaver configured to interleave address locations of bits within a matrix having a first predetermined number of rows and a second predetermined number of columns by bit reversing row indexes for the first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for the second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns; and

a decoder configured to receive and decode the turbo encoded data frames transmitted by the turbo encoder, the decoder including a de-interleaver that receives the interleaved reassembles the address locations of bits within the matrix by reversing the interleaved output of the interleaver using reverse steps of the interleaver.

14. An interleaver comprising:

an input data memory configured to store an *N* number of bits at corresponding input data memory addresses;

an interleaver matrix configured to read and store the input data memory addresses in at least a two-dimensional matrix having a first predetermined number of rows and a second predetermined number of columns, each of the rows and columns having an assigned index value;

a controller configured to set the first predetermined number of rows and the second predetermined number of rows based on the *N* number of bits using a prescribed algorithm; the controller also configured to interleave the data memory address in the interleaver matrix by bit reversing the row index values for the first predetermined number of rows and permuting the corresponding address locations of the data elements, bit reversing the column index values for the second predetermined number of columns and permuting the corresponding address locations of the data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns; the controller further configured to read out interleaved data bit addresses in the interleaver matrix column by column to produce an interleaved output read sequence;

an output buffer receiving the interleaved output read sequence from the controller, the output buffer configured to direct the input data memory to read out data bit according to the interleaved output read sequence; and

an output data memory configured to write data bits read out from the input data memory according to the interleaved output read sequence and transmit the read bits to a communication system.

15. The interleaver according to claim 14, wherein the interleaver matrix is effected within the controller.

16. The interleaver according to claim 14, wherein the controller is further configured to set the first predetermined number of rows and second predetermined number of columns to $2^m$ and $2^n$, respectively, where the values $m$ and $n$ are set such that $2^{n+m}$ is greater than or equal to the at least $N$ number of bit storage locations.

17. The interleaver according to claim 16, wherein the values of $m$ and $n$ are set such that $n$ is greater than or equal to $m$ and that the absolute value of the difference of values $m$ and $n$ is less than or equal to one.

18. The interleaver according to claim 17, wherein the controller is configured to reverse the bit storage locations for the first predetermined number of rows, reverse the bit storage locations for the second predetermined number of columns, and shift the bit storage locations of each of the second predetermined number of rows a respective predetermined number of columns for each data element when each individual data element is written to the matrix.

19. The interleaver according to claim 14, wherein the controller is configured to shift data elements in each particular row of the matrix a predetermined direction within the matrix a specified number of columns as determined by the relationship $2^m$ - (row#-1), where row# is a number of the particular row in the matrix and $2^m$ is the total number of rows in the matrix.